



The LatticeECP2™ and LatticeECP2M™ families redefine the low-cost FPGA category, with more of the best FPGA features for less. By integrating features and capabilities previously only available on higher cost / high performance FPGAs, these families expand the range of applications that can take advantage of low cost FPGAs.

Key Features

- **Optimized FPGA Architecture for Low Cost Applications**
 - Feature set optimized for high-volume, low-cost applications
 - Low cost TQFP, PQFP and BGA packaging
 - Up to 5.3Mbit Block RAM on LatticeECP2M and 1.1Mbit on LatticeECP2
- **3.125Gbps Embedded SERDES (ECP2M only)**
 - Low 100mW power per channel
 - Supports PCIexpress, Ethernet (1GbE and SGMII) plus multiple other standards
- **sysDSP Block**
 - High performance multiply, addition, subtract and accumulate
 - Support widths of up to 36x36
- **Pre-Engineered Source Synchronous I/O**
 - Simplifies implementation of interfaces such as DDR1/2, SPI4.2 and general purpose ADCs
 - Supports DDR1/2 at 400Mbps, SPI4.2 at 750Mbps and generic interfaces up to 840Mbps
- **Enhanced Configuration Options**
 - Configure from SPI, JTAG or microprocessor interfaces
 - Bitstream encryption and dual boot support
 - TransFR I/O for simple field upgrades
- **ispLeverCORE Intellectual Property**
 - Speed up your design cycle with ispLeverCORE Intellectual Property
- **ispLEVER Design Tools**
 - Easy to use SW package supports all Lattice FPGA and programmable logic devices
 - Evaluation boards available to test your FPGA designs
- **LatticeECP2/M Applications**
 - LatticeECP2/M devices are ideal for a variety of applications in cost sensitive markets such as Consumer, Automotive, Medical & Industrial, Networking and Computing

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LatticeECP2/M Evaluation Boards

Lattice has developed three evaluation boards for the LatticeECP2/M devices.

LatticeECP2 Standard Evaluation Board: This board is an efficient design that will help you quickly evaluate the LatticeECP2 FPGA on a ready-made platform. It features an LFE2-50E-6F484C FPGA Device (ECP2-50 in a 484fpBGA package), 64-bit PCI/PCI-x edge connector and form-factor, RS-232 connector, On-board Flash configuration memory, Various LEDs, switches, connectors, headers, an on-board power supply and prototype area.

LatticeECP2 Advanced Evaluation Board: This board features more advanced interfaces for system-level evaluation and development. The board includes a LFE2-50E-6F672C FPGA Device (ECP2-50 in a 672fpBGA package), Dual DDR2 SODIMM memory sockets, 10/100/1G Ethernet PHY with RJ-45 interface, SPI4.2 Tx/Rx connectors (840Mbps), along with many of the features included on the ECP2 Standard Evaluation board.

LatticeECP2M PCI Express x4 Evaluation Board: This board provides a plug in card that can be used to evaluate the ECP2M-35 in PCIexpress applications. It provides a PCIexpress X4 connector, configuration memory, power supplies, DDR SRAM, a sockatable oscillator, various LEDs and switch inputs. Demonstration driver software, an evaluation version of the ispLeverCORE PCIexpress IP core and supplied backend logic can be used to quickly evaluate this board in a PC environment.

LatticeECP2M SERDES Evaluation Board: This board can be used to evaluate the SERDES I/O of the ECP2M-35, or for use in more generalized environments. It includes SMA connectors to 4 quad-channel SERDES, a sockatable oscillator, various LEDs and switch inputs.

LatticeECP2 Selection Guide						
Device	ECP2-6	ECP2-12	ECP2-20	ECP2-35	ECP2-50	ECP2-70
LUTs (K)	6	12	21	32	48	68
Distributed RAM (Kbits)	12	24	42	64	96	136
EBR SRAM (Kbits)	55	221	276	332	387	1032
EBR SRAM Blocks	3	12	15	18	21	56
sysDSP Blocks	3	6	7	8	18	22
18x18 Multipliers	12	24	28	32	72	88
DLL + PLL	2+2	2+2	2+2	2+2	2+4	2+6
Maximum Available I/O	190	297	402	450	500	583
Packages	I/O Count					
144-pin TQFP (20 x 20 mm)	90	93				
208-pin PQFP (28 x 28 mm)		131	131			
256-ball fpBGA (17 x 17 mm)	190	193	193			
484-ball fpBGA (23 x 23 mm)		297	331	331	339	
672-ball fpBGA (27 x 27 mm)			402	450	500	500
900-ball fpBGA (31 x 31 mm)						583

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LatticeECP2M Selection Guide					
Device	ECP2M-20	ECP2M-35	ECP2M-50	ECP2M-70	ECP2M-100
SERDES Channels (Max)	4	4	8	16	16
LUTs (K)	19	34	48	67	95
Distributed RAM (Kbits)	41	71	101	145	202
EBR SRAM (Kbits)	1217	2101	4147	4534	5308
EBR SRAM Blocks	66	114	225	246	288
18x18 Multipliers	24	32	88	96	168
DLL + PLL	2+8	2+8	2+8	2+8	2+8
Maximum Available I/O	301	411	457	449	601
Packages	SERDES I/O Combinations				
256-ball fpBGA (17 x 17 mm)	4/140	4/140			
484-ball fpBGA (23 x 23 mm)	4/301	4/301	4/287		
672-ball fpBGA (27 x 27 mm)		4/411	8/387		
900-ball fpBGA (31 x 31 mm)			8/457	16/449	16/457
1156-ball fpBGA (35 x 35 mm)					16/601

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