

# PhaseLink Offices

[www.phaselink.com](http://www.phaselink.com)

## PhaseLink Corporation, USA

US Headquarters  
47745 Fremont Boulevard  
Fremont, CA 94538  
+ 1.510.492.0990 (phone)  
+ 1.510.492.0991 (fax)  
[salesinfo@phaselink.com](mailto:salesinfo@phaselink.com)

## PhaseLink Company, Ltd., Taiwan

Asia Pacific Headquarters  
5F-3, No. 94, Pao Chung Road.  
Hsin Tien, Taipei, Taiwan, R.O.C.  
+ 886.2.2910.0248 (phone)  
+ 886.2.2910.0249 (fax)  
[salesinfo.taiwan@phaselink.com](mailto:salesinfo.taiwan@phaselink.com)

## PhaseLink Technology Inc., China

Rm.1101, Building 61, No.500 Baocheng Rd.  
Minhang District, Shanghai, China 201100  
+86-21-6460-7566 (phone)  
[salesinfo.china@phaselink.com](mailto:salesinfo.china@phaselink.com)

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# Product Selector Guide

2008



CHINA ROHS



EU ROHS

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## About PhaseLink

PhaseLink is the world leader in high performance Frequency Generation and Signal Conditioning Timing Source ICs for the Consumer, Communications, and Storage Network markets.

Our expertise resides in analog intensive mixed signal integrated circuits for low-jitter and phase noise frequency synthesis, multiplication, and conditioning circuits. Through our proprietary technology, we provide unequalled performance in frequency multiplication for optical, Gigabit Ethernet, and telecommunication applications as well as the world's smallest foot-print and lowest power programmable clocks. Our constant efforts for improvement, innovation, and simplification have enabled us to deliver the highest quality and reliability products with an affordable price.

Through our advanced design, manufacturing, and packaging capabilities, coupled with our responsiveness to shifting market trends and customer demands, we have established a track record of producing high-performance, low-cost products, in an expedited manner

Our design methodology enables rapid prototyping of both standard and custom solutions, available for sampling in short lead time.

Our worldwide manufacturing information system ensures on-time delivery. Furthermore, PhaseLink and its suppliers are ISO 9001 and ISO14000 certified.

PhaseLink is proud to be financially backed by the world's three leading financial institutions, Intel, Samsung, and JAFCO.



## Frequency Generation

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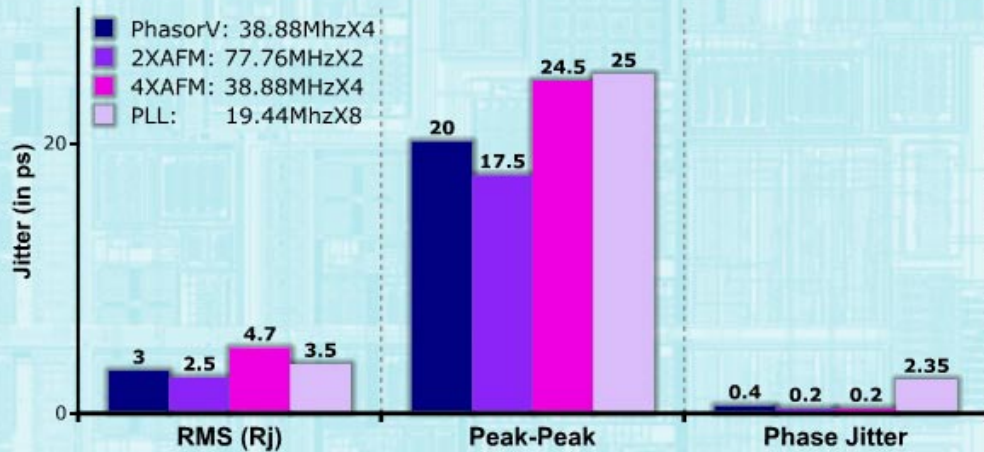
- 4 Analog Frequency Multiplier (AFM)
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# Analog Frequency Multiplier (AFM™)

## Unbeatable Performance

- < 0.25ps Phase Jitter (12KHz-20MHz)
- < 2.5ps RMS Period Jitter
- < 20ps PK-PK Period Jitter

155.52MHz Jitter Comparison



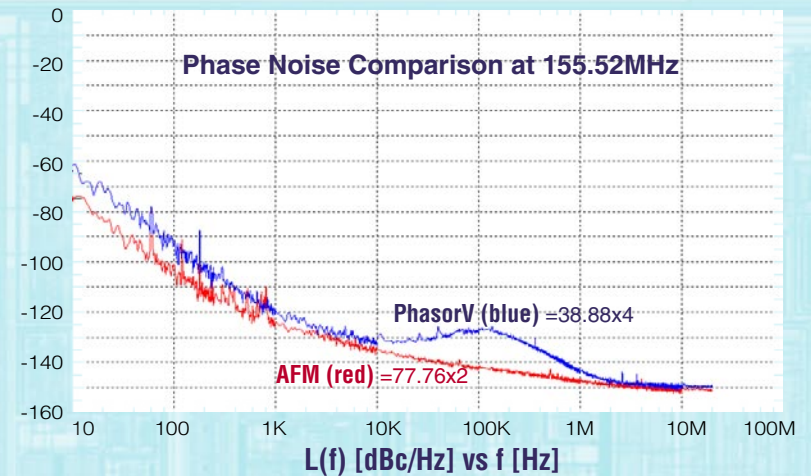
Industry's first CMOS Non-PLL multiplier utilizing analog multiplication of a high frequency fundamental or 3rd overtone crystal input. Our patented AFM technology can generate up to 800MHz in PECL, LVDS or CMOS without using a phased lock loop. This is achieved with practically no jitter or phase noise deterioration.

See page 20 for detailed product selector guide.

# PhasorV™ Frequency Multiplier

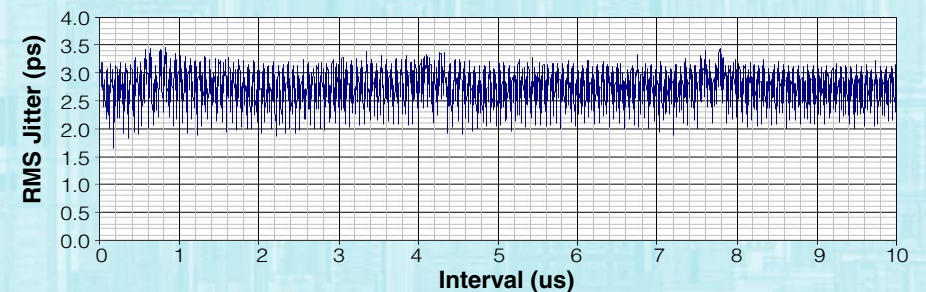
## The Best In Class Multiplier

- < 0.4ps Phase Jitter (12KHz-20MHz)
- < 20ps PK-PK Period Jitter



- Practically, No Accumulated Jitter

PhasorV Long Term Jitter  
(Crystal=38.88MHz, Output=155.52MHz)



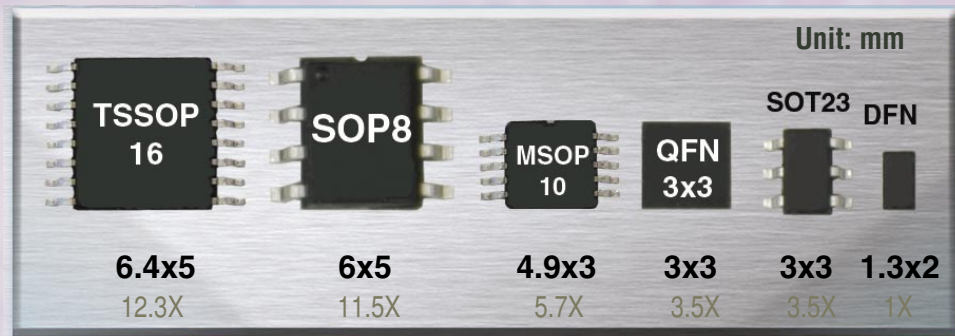
For detail product selector guide, please refer to page 21.

# Tiny Package, Big Benefits !

World's Smallest Programmable Clock



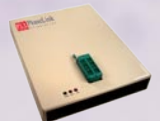
- ▶ **Lowest Power Consumption**
- ▶ **1.8V, 2.5V, 3.3V Supply**
- ▶ **30~70ps Peak-Peak Jitter**
- ▶ **Fast Turnaround with Factory Programming**



PhaseLink's PicoPLL programmable clock family is a general purpose frequency synthesizer with the key features of low jitter, low power and tiny package. This low cost frequency source solution is designed to fit almost any application where high performance, space saving and time to market is crucial.

Device Family	# of PLLs	EMI	VCXO	Input (MHz)	# of Outputs	Voltage	Package
<b>PL611s</b>	1			Crystal: 10 - 50	up to 2	1.8V, 2.5V, 3.3V	DFN, (M)SOP, SOT23, QFN3x3, (T)SSOP
<b>PL612</b>	2			Ref Clock: 0.01-200	up to 8		
<b>PL613</b>	3				up to 8		
<b>PL671</b>	1	√		Crystal: 10 - 50	up to 3	1.8V, 2.5V, 3.3V	SOT23, (M)SOP, QFN3x3, (T)SSOP
<b>PL672</b>	2				up to 10		
<b>PL673</b>	3				up to 10		
<b>PL653</b>	3		√	Crystal: 17 - 36	up to 9	2.5V, 3.3V	QFN3x3 (T)SSOP
<b>PL657</b>	3	√	√	Crystal: 17 - 36	up to 9	2.5V, 3.3V	QFN3x3 (T)SSOP

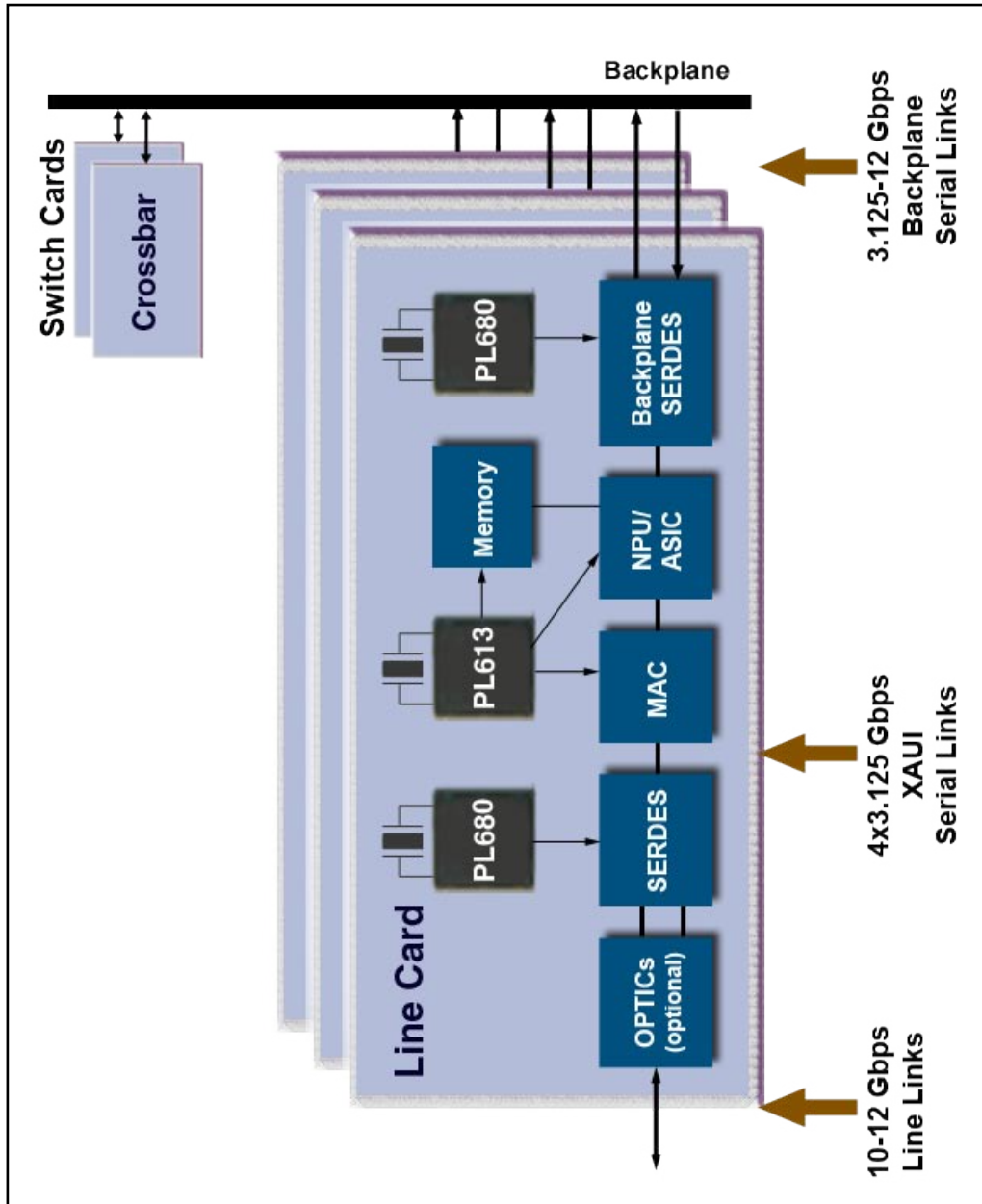
**Programming Box Available**  
Contact PhaseLink for Programming box support



## Application Examples

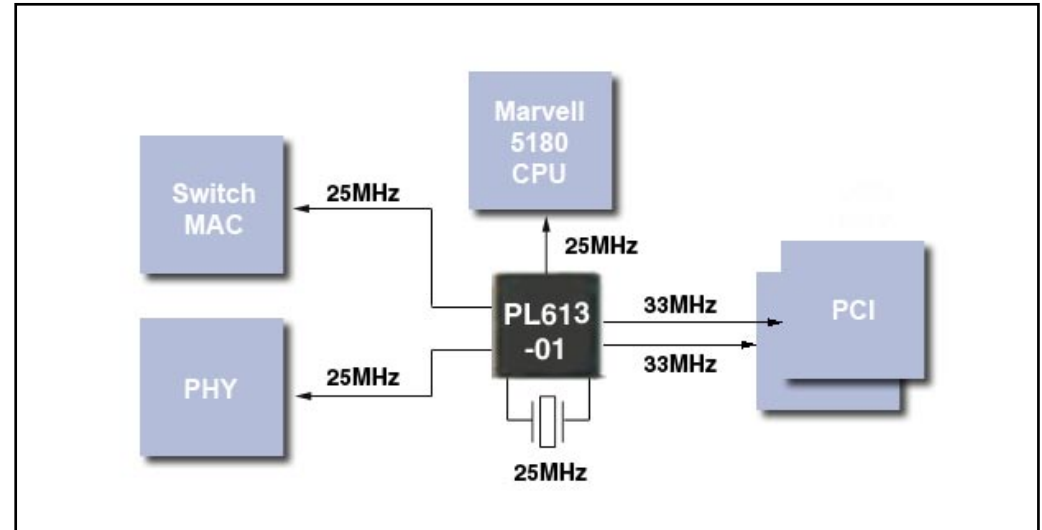
### 1. Line Card for High Speed Serial Links

PhaseLink offers a variety of high performance timing sources for the most demanding communication applications such as 10Gbps line cards.



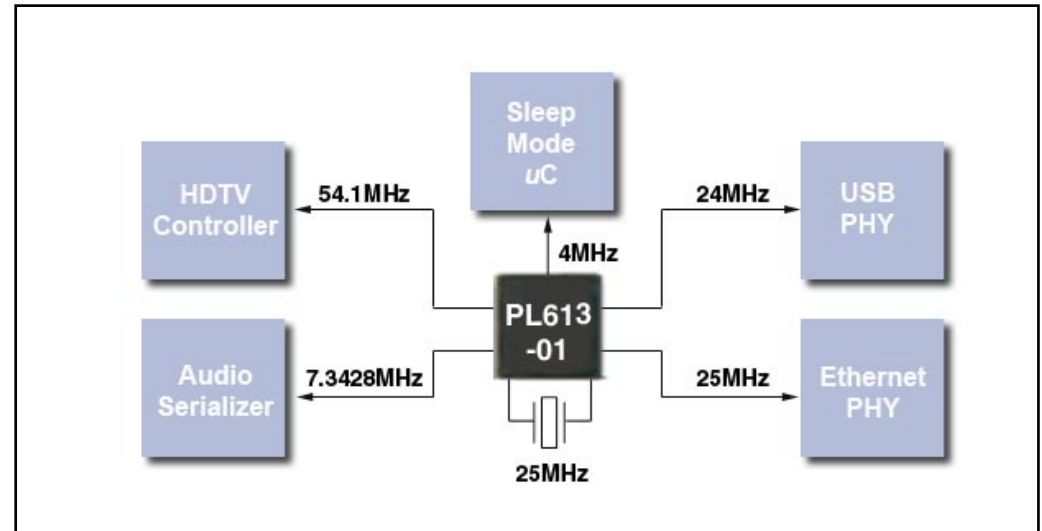
### 2. 802.11n AP Router

PL613-01, a three PLL Programmable Frequency Synthesizer, can replace multiple crystals oscillators reducing cost, size and power in AP router designs.



### 3. DTV/HDTV

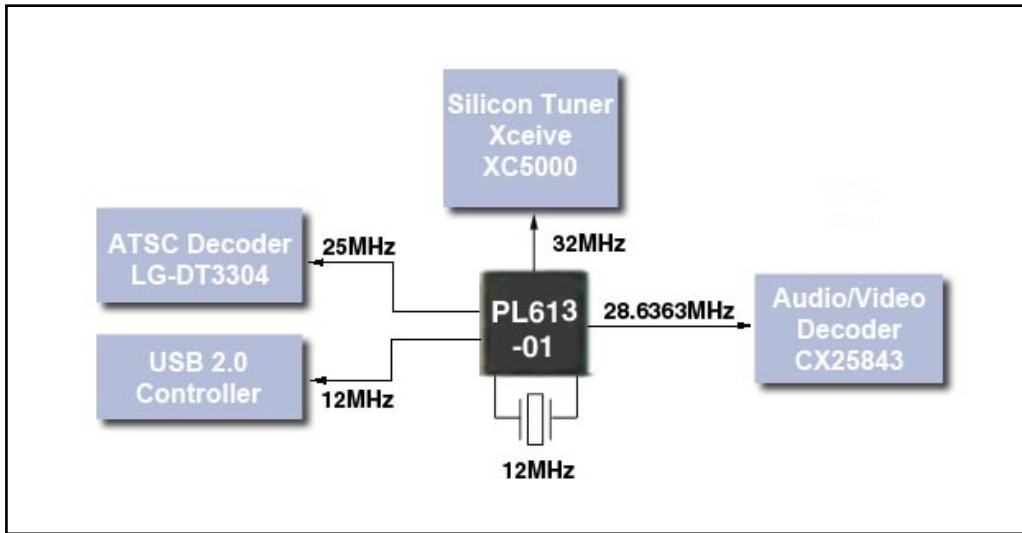
PL613-01, a three Programmable Frequency Synthesizer, provides all the necessary clocks for common DTV/HDTV requirements.



## Application Examples

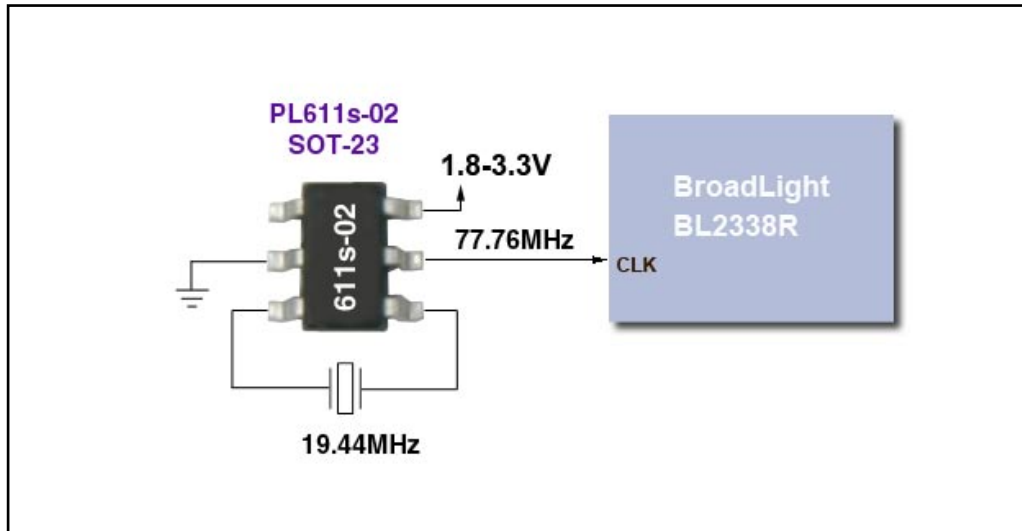
### 4. ATSC USB DVB-T

The PL613-01 provides all the clocking for complex mobile systems in a fraction of the space required by individual crystals and oscillators.



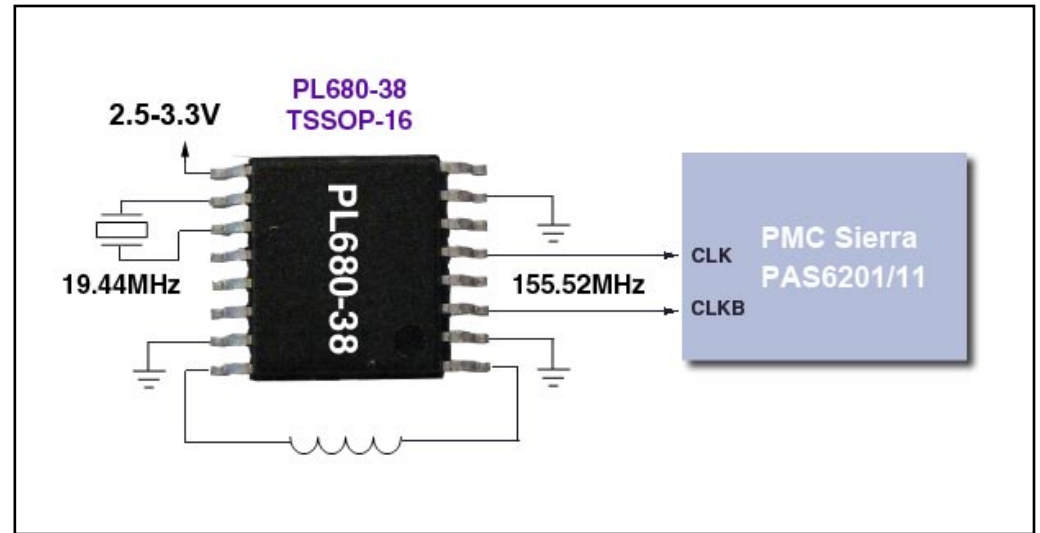
### 5. GPON (Gigabit Passive Optical Network)

Using PhaseLink's PL611s-02, customers can create high frequency and low jitter clocks by using low cost, low frequency crystals.



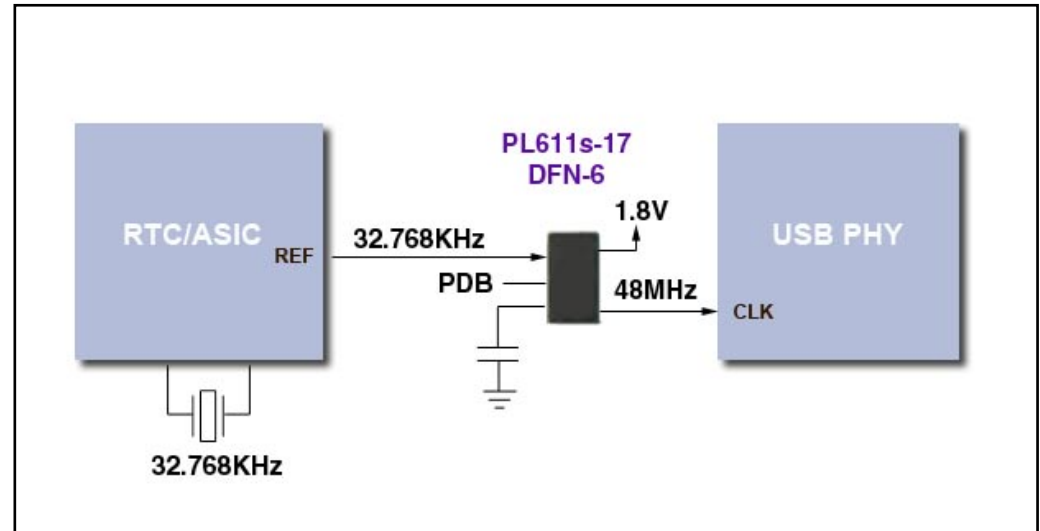
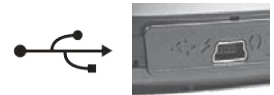
### 6. GE-PON (Gigabit Ethernet Passive Optical Network)

PL680 can create high freq. differential (LVPECL, LVDS) from low cost crystals to support low jitter requirements in communications app.



### 7. USB Clock

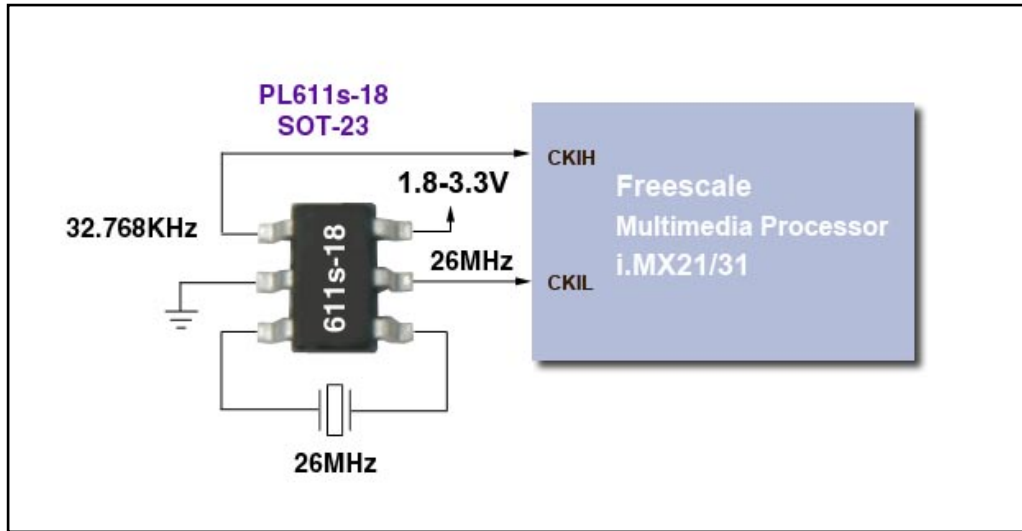
PL611s-17, a KHz to MHz Programmable Frequency Synthesizer, can generate a USB clock from a 32.768KHz reference input.



## Application Examples

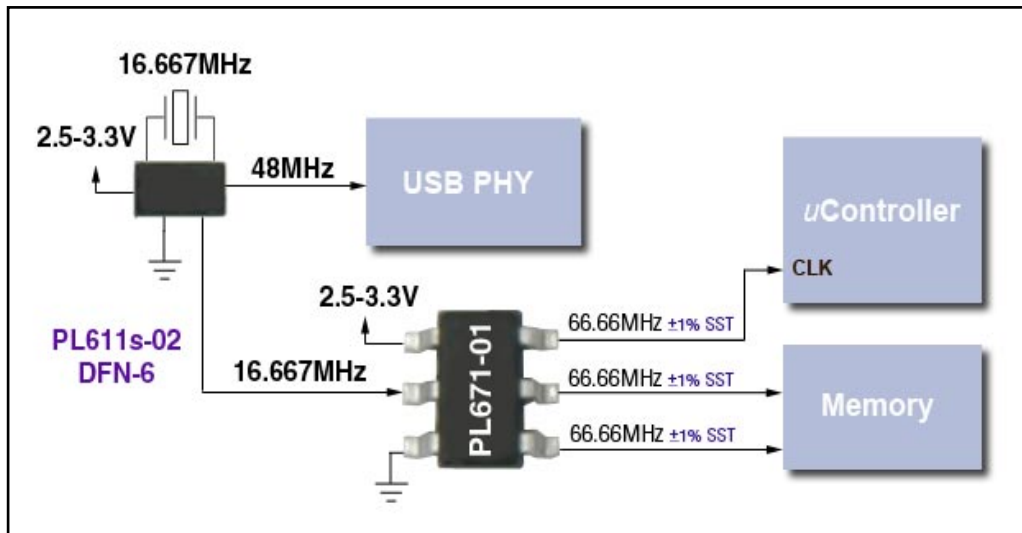
### 8. VOIP Phone

PL611s-18, a MHz to KHz Programmable Frequency Synthesizer, can generate both MHz and KHz clock outputs from a MHz crystal input.



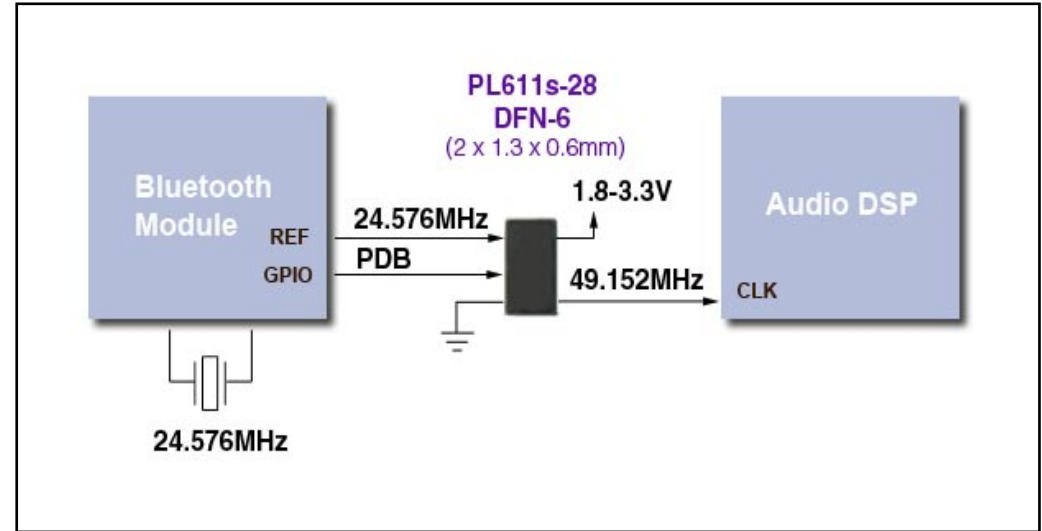
### 9. Printer

PhaseLink's PL671 PicoEMI Programmable Spread Spectrum Clock Generator (PSSCG) can generate multiple clocks to reduce EMI emission.



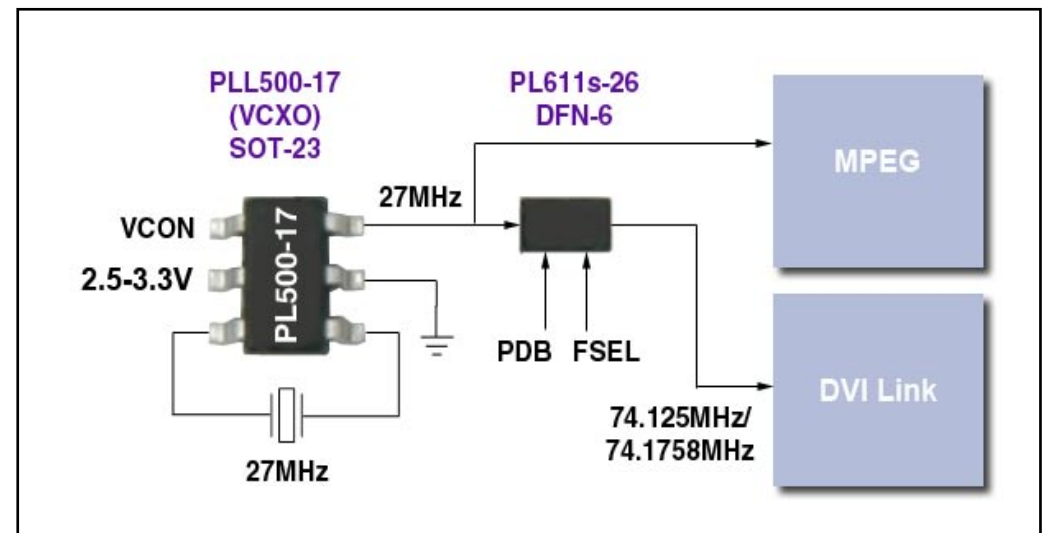
### 10. Bluetooth Headset

PL611s-28, a low power programmable PLL, is the ideal clocking solution to generate any frequency for handheld and small footprint applications.



### 11. Digital Video (Set top Box, DTV)

Using PLL500 VCXO IC and PL611s Pico-PLL programmable clock, users are able to generate multiple VCXO clocks at low cost.



## 12. Pico-EMI Clock Summary

PhaseLink's PicoEMI PL671 Programmable Spread Spectrum Clocks provide the flexibility and performance required for the most demanding EMI reduction requirements.

### EMI Reduction Starter Kit (Pre-Programmed)



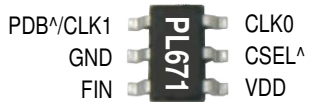
**PL671-01A/B/C/D**

Features	-01A	-01B	-01C	-01D
<b>Input (MHz)</b>	Crystal: 10-40 Ref: 10-40		Ref: 30-150	
<b>Output (MHz)</b>	CLK0 = FIN X 1			
<b>Selectable Spread Spectrum Magnitude</b>	±0.5%	-1.0%	±0.25%	-0.5%
	±1.0%	-2.0%	±0.50%	-1.0%
	±1.5%	-3.0%	±1.00%	-2.0%
	OFF	OFF	OFF	OFF

### Small Footprint: SOT23-6 Package (Programmable)



**PL671-01**



**PL671-02**

Features	PL671-01	PL671-02
<b>Input (MHz)</b>	Crystal: 10-40 Ref: 1-200	Reference: 1-200
<b>Output (MHz)</b>	Programmable up to 200MHz	
<b># of outputs</b>	Up to 2 <sup>1</sup>	Up to 2 <sup>1</sup>
<b>Spread Spectrum Magnitude<sup>2</sup></b>	Fixed	Fixed Selectable
<b>Power Down</b>	Yes <sup>1</sup>	Yes <sup>1</sup>

1: Pin 1 can be configured as PDB input or CLK output.  
2: Factory Program: Center: ±0.125~±2.0% (+0.125% step)  
Down: -0.25~ -4.0% (-0.25 step), or OFF

### SOP8/MSOP8 Package (Programmable)



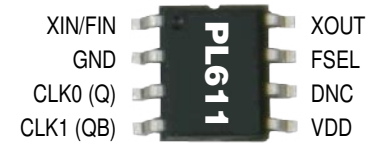
**PL671-01**

Features	PL671-01
<b>Input (MHz)</b>	Crystal: 10-40 or Ref: 1-200
<b>Output (MHz)</b>	Programmable up to 200MHz
<b># of outputs</b>	Up to 3 <sup>1</sup>
<b>Spread Spectrum Magnitude<sup>2</sup></b>	Up to 4 Fixed Selectable
<b>Power Down</b>	Yes <sup>1</sup>

1: Pin 2,6 can be configured as CLK output.  
2: Factory Program: Center: ±0.125~±2.0% (+0.125% step)  
Down: -0.25~ -4.0% (-0.25% step), or OFF

## 13. Application Specific Standard Clock for HD Video

PL611-31A/B/C/D are specially designed to support the high frequency clock requirements for HD Video applications. Utilizing a 27MHz crystal or reference clock input, this family provides selectable complementary CMOS for both US and European HD standard clock frequencies. This unique complementary CMOS output structure can clock both PECL and LVDS inputs and provide the low jitter required for video applications.



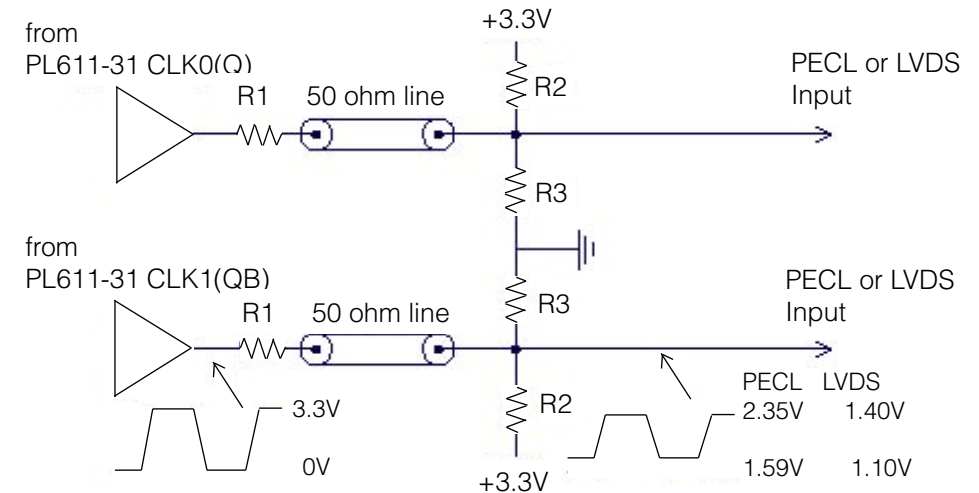
**PL611-31B/D**



**PL611-31A/C**

Features	-31A	-31B	-31C	-31D
<b>Crystal Input (MHz)</b>	-	27	-	27
<b>Ref Input (MHz)</b>	27	27	27	27
<b>PK-PK Jitter</b>	<50ps			
<b>Selectable Output Frequency (MHz) via FSEL input</b>	148.50000	74.25000		
	148.35164	74.17582		
<b>Package Type</b>	SOT6	SOP8	SOT6	SOP8

### Turning Differential CMOS output to PECL and LVDS.



For PECL input	For LVDS Input
R1 = 130 ohm	R1 = 360 ohm
R2 = 82 ohm	R2 = 82 ohm
R3 = 130 ohm	R3 = 130 ohm

Notes: 1. Place R1 as close to the CMOS outputs as possible  
2. Place R2 and R3 as close to the PECL/LVDS Inputs as possible

# Programmable Clocks

PicoPLL is PhaseLink's line of programmable, low-cost clock ICs. Accepting a single crystal or reference clock input and producing up to 10 outputs, the PicoPLL family is designed to reduce system cost and fit almost any application where high performance, low-power, space saving, cost sensitivity and time to market are crucial.

Part Number	# of PLLs	Input (MHz)		Output (MHz)	# of Outputs	Voltage			Programmable I/O Pin				Ultra Low Power	Other Features	Package
		Xtal	Reference			1.8V	2.5V	3.3V	PDB	OE	FSEL	CLK			

## MHz to MHz Clocks

<b>PL611s-02</b> <b>PL611s-28</b>	1	10 - 50	1 - 200	≤ 200 (-02) ≤ 65*1 (-28)	≤ 2	✓	✓	✓	✓	✓	✓	✓	✓	√ (-28)		DFN-6, SC70-6, SOT23-6
<b>PL611-01</b>	1	10 - 30	1 - 200	≤ 200	≤ 3		✓	✓	✓	✓	✓	✓				SOT23-6, SOP-8, MSOP-8
<b>PL611-30</b> <b>PL611-31</b>	1	10 - 30	1 - 200	≤ 400 (-30) ≤ 200 (-31)	≤ 3		✓	✓		✓	✓	✓		Differential CMOS and PECL/LVDS compatible		SOP-8, MSOP-8, SOT23-6
<b>PL611s-26</b>	1	-	1 - 200	≤ 200	≤ 2	✓	✓	✓	✓	✓	√*2	✓		Fixed FSEL Input pin		DFN-6, SC70-6, SOT23-6
<b>PL611s-27</b>	1	-	1 - 200	≤ 65*1	2	✓	✓	✓	✓	✓	✓	√*3	✓	Fixed 2nd Clock output		DFN-6, SC70-6, SOT23-6
<b>PL612-01</b>	2	10 - 50	5 - 200	≤ 200	≤ 8	✓	✓	✓	✓	✓	✓	✓	✓	Individual clock disable option for each output		QFN3x3-16, (T)SSOP-16
<b>PL613-01</b>	3	10 - 50	5 - 200	≤ 200	≤ 8		✓	✓	✓	✓		✓	✓	Individual clock disable option for each output		QFN3x3-16, (T)SSOP-16
<b>PL613-21</b>	3	10 - 50	5 - 200	32KHz, 1-200 MHz	4	✓	✓	✓					✓	Individual VDD buffer and Individual PDB control.		QFN3x3-16.
<b>PL653-01</b>	3	17 - 36		≤ 200	≤ 9		✓	✓	✓	✓	✓	✓	✓	VCXO Output		SOP-8, QFN, TSSOP

## MHz to MHz Clocks (With EMI Reduction)

<b>PL671-01</b>	1	10 - 40	1 - 200	≤ 200	≤ 3		✓	✓	✓		✓	✓		SS Rate: ±0.125%~±2.0% (C) or -0.25%~-4.0% (D)		SOT23-6, MSOP-8, SOP-8
<b>PL672-01</b>	2	10 - 50	1 - 200	≤ 200	≤ 10	✓	✓	✓	✓	✓	✓	✓		SS Rate: ±0.125%~±3.0% (C) or -0.25%~-5.0% (D)		QFN3x3-16, (T)SSOP-16/-20
<b>PL673-01</b>	3	10 - 50	1 - 200	≤ 200	≤ 10	✓	✓	✓	✓	✓	✓	✓		SS Rate: ±0.125%~±3.0% (C) or -0.25%~-5.0% (D)		QFN3x3-16, (T)SSOP-16/-20
<b>PL657-01</b>	3	17 - 36		≤ 200	≤ 9		✓	✓	✓	✓	✓	✓		VCXO with EMI reduction . SS Rate: ±0.125%~±3.0% (C) or -0.25%~-5.0% (D)		QFN3x3-16, (T)SSOP-16/-20

## KHz to MHz Clocks

<b>PL611s-17</b>	1	-	0.01 - 200	≤ 65*1	≤ 2	✓	✓	✓	✓	✓	✓	✓	✓	32.768KHz input to MHz output. (Ideal for USB Clock)		DFN-6, SC70-6, SOT23-6
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## MHz to KHz Clocks

<b>PL611s-18</b>	1	10 - 50	1 - 200	0.5KHz - 65*1	≤ 2	✓	✓	✓	✓	✓	✓	✓	✓	Ideal for generating 32.768KHz output.		DFN-6, SC70-6, SOT23-6
<b>PL611s-19</b>	1	-	1 - 200	0.5KHz - 65*1	2	✓	✓	✓	✓	✓	✓	✓	✓	Ideal for generating 32.768KHz output.		DFN-6, SC70-6, SOT23-6
<b>PL613-21</b>	3	10 - 50	1 - 200	32KHz, 1-200 MHz	4	✓	✓	✓					✓	Individual VDD buffer and Individual PDB control.		QFN3x3-16

Note \*1: Maximum output at 1.8V. \*2: Fixed FSEL Input pin. \*3: Fixed 2nd Clock output.

## Crystal Oscillator (XO) ICs

PhaseLink's crystal oscillator ICs provide the best level of negative impedance, lowest jitter, and lowest phase noise up to 200MHz. Our best in class buffer outputs (CMOS, LVDS, LVPECL) make them suitable for all types of applications, including low current, low jitter, low phase noise system clock reference, and ceramic based SMD crystal oscillators.

Part Number	Function	Input (MHz)	Output (MHz)	Output Type	Operating Voltage	Package
<b>PL610-01</b> <b>PL610-02</b> <b>PL610-03</b>	Programmable Clod, XO, Output Divider	5 - 130	0.1 - 130	CMOS	1.8V - 3.3V	DIE SOT23-6 DFN-6
<b>PL610-27</b>	XO	10 - 52	10 - 52	CMOS	1.8V - 3.3V	SOT23-6
<b>PLL600-27T</b>	XO	10 - 52	10 - 52	3 CMOS	1.8V - 3.3V	SOP-8
<b>PLL620-20</b>	XO	100 - 200	100 - 200	PECL/LVDS	2.5V, 3.3V	DIE
<b>PLL620-30</b>	XO	65 - 130	32.5 - 130	PECL/LVDS	2.5V, 3.3V	DIE
<b>PLL620-38</b> <b>PLL620-39</b>	XO	65 - 130	32.5 - 130	PECL (-38) LVDS (-39)	2.5V, 3.3V	TSSOP-16
<b>PLL620-80</b>	XO	19 - 65	9.5 - 65	PECL, LVDS	2.5V, 3.3V	DIE
<b>PLL620-88</b> <b>PLL620-89</b>	XO	19 - 65	9.5 - 65	PECL (-88) LVDS (-89)	2.5V, 3.3V	TSSOP-16

## General Purpose PLL Multiplier Clocks

Integrating with the best in class PLL multiplier, this high performance clock family products offer very low jitter output frequency from 750KHz to 800MHz using a low-cost crystal input. Ideas for all types of applications to replace multiple expensive crystals or crystal oscillators.

Part Number	Function	Input (MHz)	Multiplier	Output (MHz)	Output Type	Voltage	Package
<b>PLL602-00</b>	XO+PLL	12 - 25	1,2,4,8	12 - 200	CMOS	3.3V	DIE, WAFER
<b>PLL602-35</b>	XO+PLL	12 - 25	/16 to x32	0.75 - 800	PECL, Inverted OE	3.3V	TSSOP-16, QFN3x3-16
<b>PLL602-37</b> <b>PLL602-38</b> <b>PLL602-39</b>	XO+PLL	12 - 25	/16 to x32	0.75 - 800	CMOS (-37) PECL (-38) LVDS (-39)	3.3V	TSSOP-16, QFN3x3-16
<b>PLL620-00</b>	XO+PLL	100-200	1,2,4	100 - 800	PECL, LVDS CMOS	3.3V	DIE, WAFER
<b>PLL620-07</b> <b>PLL620-08</b> <b>PLL620-09</b>	XO+PLL	100-200	1,2,4	100 - 800	CMOS (-07) PECL (-08) LVDS (-09)	3.3V	TSSOP-16, QFN3x3-16

## VCXO (Voltage Controlled Crystal Oscillator) ICs

PhaseLink's integrated low phase noise VCXO products provide cost efficient solutions with high linearity, wide pull-range, and very high temperature stability. They are available in die form or in small form factor packaged chips. Our products meet performance requirements of SONET, ADSL, VDSL, Set top box, and many more applications.

Part Number	Function	Input (MHz)	Multiplier	Output (MHz)	Output Type	Pull Range (ppm) <sup>1</sup>	Voltage	Package
<b>PLL500-15</b> <b>PLL500-16</b> <b>PLL500-17</b>	VCXO	17 - 36	N/A	1 - 4.5 4 - 18 17 - 36	CMOS	+/-200	2.5-3.3V	DIE, SOT23-6 SOP-8
<b>PLL500-17B</b> <b>PLL500-27B</b> <b>PLL500-37B</b>	VCXO	17 - 36 27 - 65 65 - 130	N/A	17 - 36 27 - 65 65 - 130	CMOS	+/-150	2.5-3.3V	DIE, SOP-8
<b>PLL520-20</b>	VCXO	120 - 200	N/A	120 - 200	CMOS PECL LVDS	+/-110	3.3V	DIE
<b>PLL520-30</b>	VCXO	65 - 130	N/A	32.5 - 130	PECL LVDS	+/-120	2.5-3.3V	DIE
<b>PLL520-38/39</b>	VCXO	65 - 130	N/A	32.5 - 130	PECL LVDS	+/-120	2.5-3.3V	TSSOP-16
<b>PLL520-80</b>	VCXO	19 - 65	N/A	9.5 - 65	PECL LVDS	+/-200	2.5-3.3V	DIE
<b>PLL520-88/89</b>	VCXO	19 - 65	N/A	9.5 - 65	PECL LVDS	+/-200	2.5-3.3V	TSSOP-16
<b>PLL521-23</b>	VCXO	100 - 200	N/A	100 - 200	PECL	+/-110	2.5-3.3V	TSSOP-16 DIE
<b>PLL502-00</b>	VCXO+PLL	12 - 25	1,2,4,8	12 - 200	CMOS	+/- 200	3.3V	DIE
<b>PLL502-02</b>	VCXO+PLL	12 - 25	2	24 - 50	CMOS	+/- 200	3.3V	SOP-8
<b>PLL502-03</b>	VCXO+PLL	12 - 25	4	48 - 100	CMOS	+/- 200	3.3V	SOP-8
<b>PLL502-04</b>	VCXO+PLL	12 - 25	8	96 - 200	CMOS	+/- 200	3.3V	SOP-8
<b>PLL502-30</b>	VCXO+PLL	12 - 25	/16 to x32	0.75 - 800	CMOS PECL LVDS	+/- 200	3.3V	DIE
<b>PLL502-37</b> <b>PLL502-35/38</b> <b>PLL502-39</b>	VCXO+PLL	12 - 25	/16 to x32	0.75 - 800	CMOS PECL LVDS	+/- 200	3.3V	QFN3x3-16 TSSOP-16
<b>PLL520-00</b> <b>PLL520-08</b> <b>PLL520-09</b>	VCXO+PLL	100 - 200	1,2,4,8	100 - 800	CMOS PECL LVDS	+/- 110	3.3V	DIE QFN3x3-16 TSSOP-16
<b>PLL520-10</b>	VCXO+PLL	65 - 130	1,2,4,8	65 - 800	CMOS PECL LVDS	+/- 110	3.3V	DIE

## Analog Frequency (non-PLL) Multiplier (AFM™)

PhaseLink's low phase noise and low jitter Analog Frequency Multiplier products provide the most cost efficient clocking solutions for high speed applications. The multiplication of two (X2) or four (X4) times the input crystal frequency significantly lower the cost of expensive crystals to achieve the most stringent performance requirements of telecommunications, storage networking, and high speed networking LAN systems.

Part Number	Input Range (MHz)	Output Range (MHz)	Output Type	Voltage	Jitter <sup>2</sup> (ps) - Typical			Package
					RMS Period	Peak to Peak Period	Phase Jitter <sup>1</sup> 12K-20MHz	

### VCXO ICs (AFM)

<b>PL560-08</b> <b>PL560-09</b>	75 - 200	300 - 800 (4X)	PECL (-08) LVDS (-09)	2.5V, 3.3V	4	25	0.08 @622M	DIE, Wafer QFN3x3-16 TSSOP-16
<b>PL560-37</b> <b>PL560-38</b> <b>PL560-39</b>	30 - 80	120 - 320 (4X)	CMOS (-37) PECL (-38) LVDS (-39)	2.5V, 3.3V	4.7	25	0.25 @155M	DIE, Wafer QFN3x3-16 TSSOP-16
<b>PL560-47</b> <b>PL560-48</b> <b>PL560-49</b>	30 - 80	60 - 160 (2X)	CMOS (-47) PECL (-48) LVDS (-49)	2.5V, 3.3V	2.5	18	0.25 @155M	DIE, Wafer QFN3x3-16 TSSOP-16
<b>PL560-68</b> <b>PL560-69</b>	75 - 200	150 - 400 (2X)	PECL (-68) LVDS (-69)	2.5V, 3.3V	2.5	18	0.10 @311M	DIE, Wafer QFN3x3-16 TSSOP-16

### XO ICs (AFM)

<b>PL663-07</b> <b>PL663-08</b>	30 - 80 (or 3rd OT)	60 - 160 (2X)	CMOS (-07) PECL (-08)	2.5V, 3.3V	2.5	18	0.29 @106M	DIE, Wafer QFN3x3-16 TSSOP-16
<b>PL663-17</b> <b>PL663-18</b> <b>PL663-19</b>	75 - 140 (or 3rd OT)	150 - 280 (2X)	CMOS (-17) PECL (-18) LVDS (-19)	2.5V, 3.3V	2.5	18	0.14 @212M	DIE, Wafer QFN3x3-16 TSSOP-16
<b>PL663-28</b> <b>PL663-29</b>	140 - 160 (or 3rd OT)	280 - 320 (2X)	PECL (-28) LVDS (-29)	2.5V, 3.3V	2.5	18	0.13 @311M	DIE, Wafer QFN3x3-16 TSSOP-16

Note1: Phase Noise was obtained using Agilent E5500 data.

Note2: No Filtering was used in Jitter Calculations.

## PhasorV™ Frequency Multiplier

The PhasorV is a low jitter and low phase noise frequency multiplier, capable of 0.4ps RMS phase jitter and less than 25ps peak to peak period jitter, with practically no Accumulated Jitter. Using a low-cost crystal of 19-40MHz, the PhasorV enables output frequencies of 2X, 4X, 8X, or 16X, up to 640MHz. It supports CMOS, LVDS, and PECL outputs.

Part Number	Input Range (MHz)	Output Range (MHz)	Output Type	# Of Output	Voltage	Jitter <sup>2</sup> (ps) - Typical			Package
						RMS Period	Peak to Peak Period	Phase Jitter <sup>1</sup> 12K-20MHz	

### VCXO ICs

<b>PL580-30</b>	19 - 40	38 - 640 (2X, 4X, 8X, 16 X)	CMOS, PECL, LVDS	1	3.3V	3	20	0.4 @155M	DIE Wafer
<b>PL580-37</b> <b>PL580-38</b> <b>PL580-39</b>	19 - 40	38 - 320 (2X, 4X, 8X)	CMOS (-37) PECL (-38) LVDS (-39)	1	3.3V	3	20	0.4 @155M	QFN3x3-16 TSSOP-16
<b>PL580-68</b> <b>PL580-69</b>	20 - 40	320 - 640 (16X)	PECL (-68) LVDS (-69)	1	3.3V	6	40	0.4 @622M	QFN3x3-16 TSSOP-16

### XO ICs

<b>PL680-30</b>	19 - 40	38 - 640 (2X, 4X, 8X, 16 X)	CMOS, PECL, LVDS	1	2.5V, 3.3V	3	20	0.4 @155M	DIE Wafer
<b>PL680-37</b> <b>PL680-38</b> <b>PL680-39</b>	19 - 40	38 - 640 (2X, 4X, 8X, 16 X)	CMOS (-37) PECL (-38) LVDS (-39)	1	2.5V, 3.3V	3	20	0.4 @155M	QFN3x3-16 TSSOP-16
<b>PL685-38</b> <sup>3</sup>	19 - 50	50 - 800	PECL	1	2.5V, 3.3V	TBD	TBD	TBD	QFN3x3-16 TSSOP-16
<b>PL685-39</b> <sup>3</sup>	19 - 50	50 - 800	LVDS	1	2.5V, 3.3V	TBD	TBD	TBD	QFN3x3-16 TSSOP-16

Note1: Phase Noise was obtained using Agilent E5500 data.

Note2: No Filtering was used in Jitter Calculations.

Note3: Contact Factory for availability.

## EMI Reduction ICs

PhaseLink's proprietary Spread Spectrum Timing (SST) technology can efficiently suppress EMI without requiring expensive enclosures or system redesign. These EMI reduction ICs with very low cycle to cycle jitter (100ps Peak-Peak) are suitable for clock generation from a single crystal or a signal reference.

Part Number	Function	Input (MHz)	Output (MHz)	SST Modulation Magnitude	Voltage /Output	Package
<b>PL671</b> <b>PL672</b> <b>PL673</b> <b>PL657</b>	Please refer to Page 14, 16 for detailed Programmable EMI Clock information.				2.5V, 3.3V	SOT23-6, (M)SOP8, QFN3x3-16 (T)SSOP-16
<b>PLL702-01</b>	Fixed Freq. Output + SST	14.318	7 outputs out of 9 freq, <133	-0.5% to -1.25% Down Spread	3.3V	SSOP-28
<b>PLL701-21</b>	1X PLL + SST	24 - 200 Clock input	24 - 200	0.25% to 2.5% Center Spread	3.3V	SOP-8
<b>PLL701-25</b>	1X PLL + SST	33 - 90 Clock input	33 - 90 5 outputs	+/- 0.50% Center Spread	3.3V	SOP-8
<b>PLL701-26</b>	1X PLL + SST	33 - 90 Clock input	33 - 90 5 outputs	+/- 1.0% Center Spread	3.3V	SOP-8

## Multimedia Clock

PhaseLink's Multimedia Clocks are designed to provide the necessary video or audio clocking requirements.

Part Number	Input (MHz)	[Output Frequencies (MHz)] X number of outputs	Output Type	Voltage	Package
<b>PL612</b> <b>PL613</b>	Please refer to Page 16-17 for detailed Programmable Clock Information.		CMOS	1.8V 2.5V 3.3V	QFN3x3 (T)SSOP
<b>PLL650-03</b>	25	50x4, [25,100]x1, [66.6,75,83.3,100]x1, SST	CMOS	3.3V	SOP-16
<b>PLL601-22</b>	27	27x2, 1x Selectable Audio: [8.192, 11.2896, 12.288, 16.9344, 18.432, 22.5792, 8, 24.576]	CMOS	3.3V	SOP-16
<b>PLL650-04</b>	25	25x1, 50x1, [90,100,125,133,145,150] x5, SST	CMOS	3.3V	SSOP-20
<b>PLL601-27B</b>	27	Selectable Audio: [8.192, 11.2896, 12.288, 24.576]	CMOS	3.3V	SOP-8
<b>PL611-31A</b> <b>PL611-31B</b> <b>PL611-31C</b> <b>PL611-31D</b>	27	-31A/-31B: Selectable [148.5, 148.35164] -31C/-31D: Selectable [74.25/74.17582]	CMOS <sup>1</sup> PECL <sup>1</sup> LVDS <sup>1</sup>	2.5- 3.3V	SOP-8 SOT23-6

Note1: Please refer to Page 15 on how to turn differential CMOS to PECL and LVDS.

## Clock Distribution

PhaseLink's clock distribution products consist of translator buffers, zero delay buffers and non-PLL fanout buffers. These general purpose buffer products will reproduce a master clock frequency up to 1GHz with low skew between the outputs. Our zero delay buffers use a phase locked loop to ensure zero-delay between the outputs and the master signal.

### ► Translator Buffers

Part Number	Function	Input/Output (MHz)	Output Type	Description	Voltage	Package
<b>PLL130-05</b>	Translator to PECL	DC to 1000	1 PECL	Single ended to PECL, OE (Low)	2.5V, 3.3V	QFN3x3-16
<b>PLL130-07</b>	Translator to CMOS	DC to 200	CMOS	Singled ended to CMOS	2.5V, 3.3V	SOP-8, QFN3x3-16
<b>PLL130-08</b> <b>PLL130-09</b>	Translator to PECL or LVDS	DC to 1000	1 PECL (-08) 1 LVDS (-09)	Single ended to PECL (-08), LVDS (-09)	2.5V, 3.3V	SOP-8, QFN3x3-16

### ► Zero Delay Buffers (ZDB)

Part Number	Function	Input/Output (MHz)	Description	Voltage	Package
<b>PL123-05(H)</b> <b>PL123S-05(H)</b> <b>PL123E-05(H)</b>	5 outputs	10-134 10-134 10-220	(H): High Drive buffer (S): Spread Spectrum Compatible (E): High speed enhanced	2.5V 3.3V	SOP-8
<b>PL123-09(H)</b> <b>PL123S-09(H)</b> <b>PL123E-09(H)</b>	9 outputs	10-134 10-134 10-220	(H): High Drive buffer (S): Spread Spectrum Compatible (E): High speed enhanced	2.5V 3.3V	TSSOP-16
<b>PLL102-03</b>	5 outputs	75-180	High Speed ZDB	3.3V	SOP-8
<b>PLL102-10</b>	3 outputs	15-120	High Performance Low Skew Buffer	2.5V 3.3V	SOT23-6 SOP-8

### ► Non-PLL Fanout Buffers

Part Number	Function	Input/Output (MHz)	Description	Voltage	Package
<b>PL103-04</b>	4 outputs	Crystal: 10-50 Ref: 1-200	Crystal or Reference input with individual OE input control	1.8-3.3V	QFN3x3, TSSOP-16
<b>PL103-06</b>	6 outputs	Crystal: 10-50 Ref: 1-200	Crystal or Reference input with PDB input.	1.8-3.3V	QFN3x3, TSSOP-16
<b>PLL600-27T</b>	3 Outputs	Crystal: 10-52 Ref: 1-100	Crystal or Reference input	1.8-3.3V	SOP-8 SOT23-6
<b>PL611-01</b>	3 Outputs	Crystal: 10-30 Ref: 1-200	Crystal or Reference input with Programmable Drive Strength.	2.5V, 3.3V	SOP-8