

Analog Peripherals

10-Bit ADC

- Programmable throughput up to 200 ksps
- Up to 16 external inputs; programmable as single-ended or differential
- Reference from internal V_{REF} , V_{DD} , or external pin
- Internal or external start of conversion sources
- Built-in temperature sensor

10-bit DAC (Current Mode)

Comparator

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Supply Voltage: 2.7 to 3.6 V

Temperature Range: -40 to +85 °C

High-Speed 8051 μ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

Memory

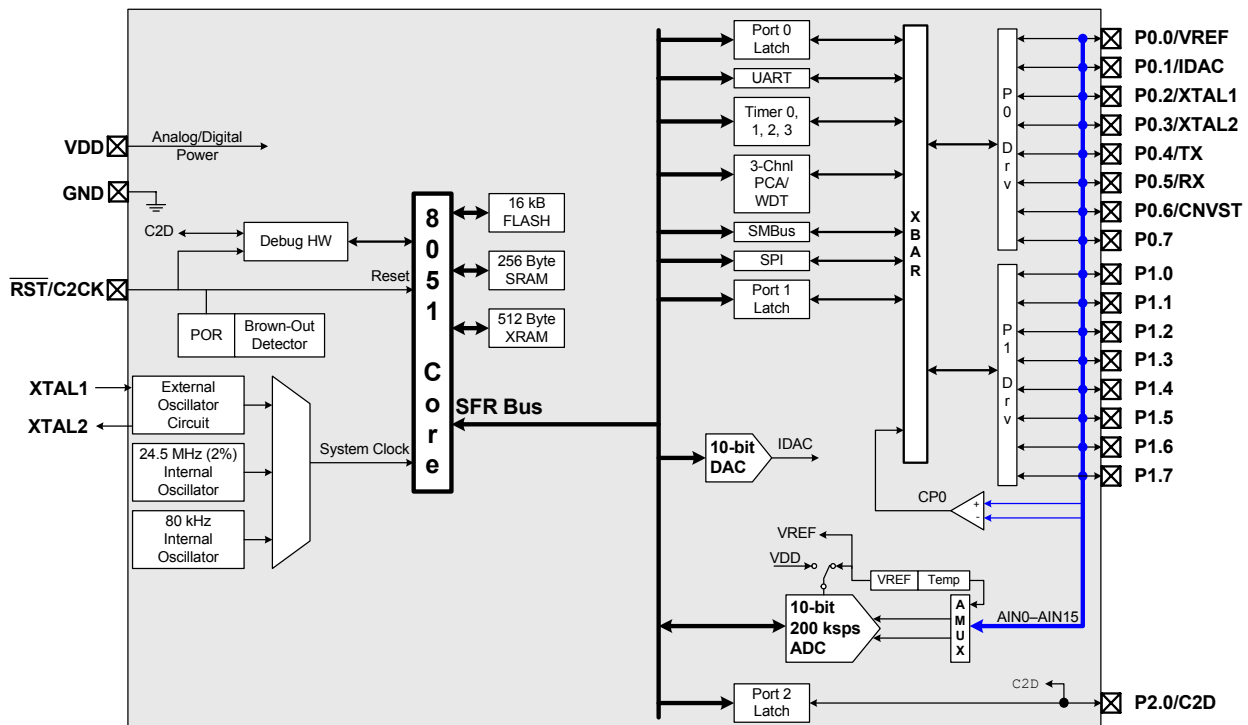
- 768 bytes data RAM
- 16 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

Digital Peripherals

- Up to 21 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I²C™ compatible), SPI™, and crystalless-UART serial ports available concurrently
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Timer with real-time clock mode
- Clock sources
 - Two internal oscillators:
 - Precision 24.5 MHz, 2% accuracy over V_{DD} and temperature
 - 80 kHz low frequency, low-power
 - External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly
- Suspend mode for maximum power savings with fast wake-up (<1 us)

Package

- 20-pin QFN
- Pin compatible with C8051F33x family of devices

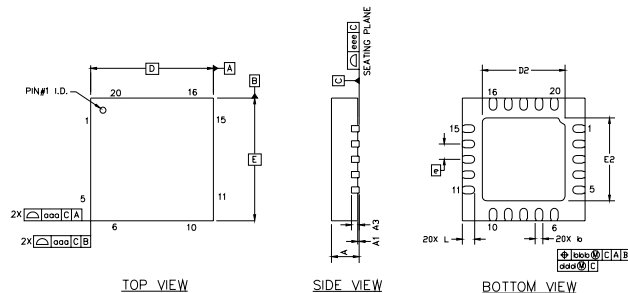


Selected Electrical Specifications

($T_A = -40$ to $+85$ °C, $V_{DD} = 2.7$ V unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Global Characteristics					
Supply Voltage				3.6	V
Supply Current with CPU Active	Clock = 25 MHz	—	TBD	—	mA
	Clock = 1 MHz	—	TBD	—	mA
	Clock = 80 kHz; V_{DD} monitor disabled	—	TBD	—	μ A
	Clock = 32 kHz; V_{DD} monitor disabled	—	TBD	—	μ A
Supply Current (shutdown)	Oscillator off; V_{DD} monitor disabled	—	TBD	—	μ A
Clock Frequency Range			—	25	MHz
Internal Oscillators					
Frequency (OSC0)			24.5	25.0	MHz
Frequency (OSC1)			80	—	kHz
A/D Converter					
Resolution					bits
Integral Nonlinearity			$\pm 1/2$	TBD	LSB
Differential Nonlinearity	Guaranteed monotonic	—	$\pm 1/2$	TBD	LSB
Signal-to-Noise Plus Distortion			55.5	—	dB
Throughput Rate			—	200	ksps
Input Voltage Range			—	V_{REF}	V
D/A Converter					
Resolution					bits
Integral Nonlinearity			$\pm 1/2$	—	LSB
Differential Nonlinearity	Guaranteed monotonic	—	$\pm 1/2$	TBD	LSB
Output Settling Time			5	—	μ s
Comparator					
Response Time Mode0	(CP+) – (CP–) = 100 mV	—	TBD	—	μ s
Current Consumption Mode0			TBD	—	μ A
Response Time Mode1	(CP+) – (CP–) = 100 mV	—	TBD	—	μ s
Current Consumption Mode1			TBD	—	μ A
Response Time Mode2	(CP+) – (CP–) = 100 mV	—	TBD	—	μ s
Current Consumption Mode2			TBD	—	μ A
Response Time Mode3	(CP+) – (CP–) = 100 mV	—	TBD	—	μ s
Current Consumption Mode3			TBD	—	μ A

QFN-20 Package Information



Dimension	Millimeters			Dimension	Millimeters		
	Min	Nom	Max		Min	Nom	Max
A	0.80	0.90	1.00	E	4.00 BSC.		
A1	0.03	0.07	0.11	E2	2.55	2.70	2.85
A3	0.25 REF			L	0.30	0.40	0.50
b	0.18	0.25	0.30	aaa	—	—	0.15
D	4.00 BSC.			bbb	—	—	0.10
D2	2.55	2.70	2.85	ddd	—	—	0.05
e	0.50 BSC.			eee	—	—	0.08

C8051F336DK Development Kit

