

## Silicon

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The XS1 family implements the XMOS XS1 architecture based on the XS1 XCore processor. Each XS1 XCore executes up to eight threads concurrently, at a speed of up to 400 MIPS. A thread has a dedicated register set enabling it to operate as a logical core. The eight threads share a single 64 KByte unified memory with no access collisions. Integer and fixed point operations are provided for efficient DSP and cryptographic operations.

Each XS1 XCore has 64 I/O pins that are programmed from software. Thread execution is deterministic and hence each thread can implement a hard real-time I/O task, regardless of the behaviour of other threads. I/O pins are grouped into logical ports of width 1, 4, 8, 16 and 32 bits. Each port incorporates serialisation/deserialisation, synchronisation with the external interface, and precision timing. Each XCore incorporates eight timers that measure time relative to a 100 MHz reference clock.

Each XS1 XCore can be connected to a switch via four internal *XMOS Links*. Each link is capable of transferring data at 800 Mbits/second. The switch provides full connectivity between the cores on the chip, and also provides up to sixteen *XMOS Links* that can transfer data at up to 400 Mbits/second.

### XS1-G4: 4-core processor



The XS1-G4 has four XCore tiles with up to 32 software threads, 1600 total MIPS, 256 KBytes of single cycle memory and a high performance switch interconnect.

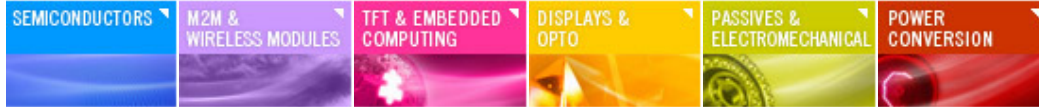
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### XS1-G2: 2-core processor



The XS1-G2 has two XCore tiles with up to 16 software threads, 800 total MIPS, 128 KBytes of single cycle memory and a high performance switch interconnect.

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## XS1-L1: 1-core processor



The energy-efficient XS1-L1 has one XCore tile with up to eight software threads, 400 total MIPS and 64 KBytes of single cycle memory.

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