

DISCOVER EVENT-DRIVEN PROCESSORS

The XS1 family of devices feature a multi-threaded processor architecture constructed from XCore™ processors connected by communication links. The architecture is scalable and any number of XCore™ processors can be connected together. The family contains the high-performance G-series and the energy-efficient L-series.

Applications are developed using a combination of XC, C and C++. XC provides extensions to C that simplify the control over concurrency, I/O and time. These extensions map directly to XS1 device resources making it easy to write embedded applications that require a blend of control code, DSP and interfacing.

Typical applications include active speakers/soundbars, USB2 audio interfaces, digital/audio ethernet systems, networked LED displays and motion control.

Performance

- Devices with one to four XCore™ event-driven processors each providing up to 400 MIPS* with up to eight concurrent, deterministic real-time threads
- 64KBytes single-cycle SRAM per XCore™ for code and data storage
- Support for high performance DSP (32 x 32 → 64bit MAC) and cryptographic functions

Responsive

- Up to 64 I/O pins per processor core
- I/O pins can be sampled or driven using a single instruction
- Data rates controlled by timers or clocks
- Supports state machines in software, fast enough to implement hardware interfaces

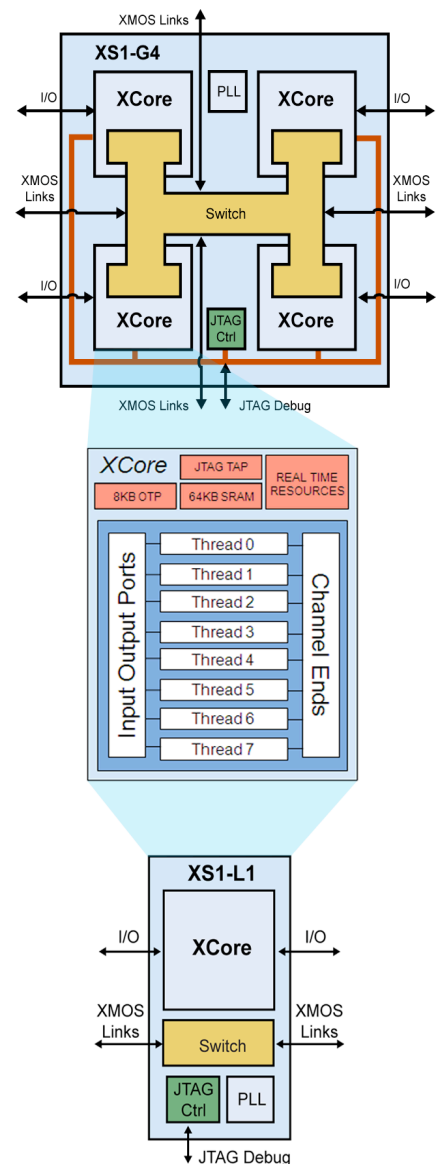
Easy-to-use

- On-chip channels provide scalable communication with other threads and cores, on- or off-chip
- Designs implemented a software-based design flow
- GUI development environment or command line tools, Windows/Linux/Mac platforms
- A range of low cost package designs for simple PCBs

Secure

- 8KBytes OTP memory per XCore for secure booting or data storage
- Protect your IP from cloning or reverse engineering

*XS1-L1 devices are available at two speed grades: '4' – 400 MIPS and '5' – 500 MIPS



FAMILY LINE-UP

The XS-1 family is available in a range of densities from one to four XCores™ providing development opportunities for a wide range of scalable embedded systems.

XS1-G devices are fabricated on TSMC's 90nm process technology and allow larger systems to be contained in a single chip.

The 65nm XS1-L devices are optimized for low power while still delivering a significant amount of processing performance for DSP, interfacing and general processing tasks.

Device	XS1-L1	XS1_L2	XS1-G2	XS1-G4
XCores	1	2	2	4
Threads	8	16	16	32
MIPS (max)	400/500	800	800	1600
SRAM (total)	64 KBytes	128 KBytes	128 KBytes	256 KBytes
OTP (total)	8 KBytes	16 KBytes	16 KBytes	32 KBytes
I/O	3v3	3v3	3v3 (5v tolerant)	3v3 (5v tolerant)
Power consumption	15-200mW	30-400mW	200-700mW	200-1200mW
Packages (I/O)	QFP64 (36) QFP128 (64)	QFN124 (84)	BGA144 (88)	BGA144 (88) BGA512 (256)

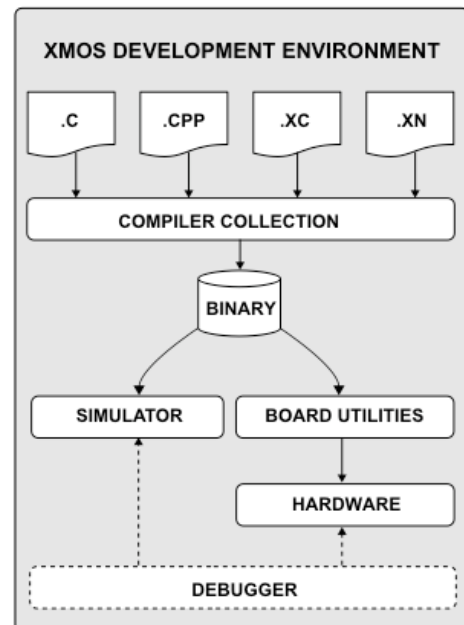
SOFTWARE DEVELOPMENT TOOLS

XMOS provides free development tools to take your XS1 powered product from concept to volume production.

The tools are based on a standard embedded software flow that supports C, C++ and XC. As well as providing compilers and a debugger, the tools validate that hard real-time constraints are met on your target device. Utilities to deploy program images onto flash memory during device manufacture, and to upgrade them in-field, are also included.

Designed to be intuitive and easy to use, you can drive the tools from an Eclipse-based GUI or the command line.

The tools are available on Windows, Mac and Linux platforms.



XMOS DEVELOPMENT KITS AND REFERENCE DESIGNS

XMOS provides a range of development boards to help you evaluate the features and capabilities of XS1 devices. Application-specific reference designs can also be licensed from XMOS.

For more information about XMOS processors, development kits and the free development tools, please visit www.xmos.com.